SN74LS112N

Product Introduction

The SN74LS112N is a Dual J-K Negative-edge-triggered Flip-Flops (with Preset and Clear).

Product Features

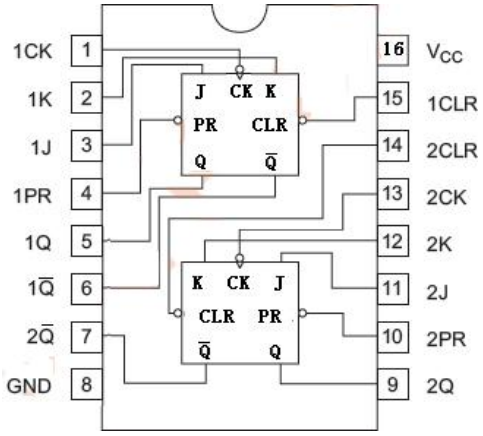
- Dual J-K Negative-edge-triggered Flip-Flopsx
- Fully compatible with TTL/DTL input and output logic level
- JK trigger with Preset and Clear
- Package : DIP16, SOP16

Product Applications

- Digital logic driver
- Industrial control applications
- Other application areasBattery-powered equipment

Package and Pin Assignment

SOP16 or DIP16.			
Pin NO	Pin Definition	Pin NO	Pin Definition
1	Input 1CK	16	Supply VCC
2	Input 1K	15	Input 1CLR
3	Input 1J	14	Input 2CLR
4	Input 1PR	13	Input 2CK
5	Output 1Q	12	Input 2K
6	Output 1$\overline{Q}$	11	Input 2J
7	Output 2Q	10	Input 2PR
8	Supply GND	9	Output 2Q

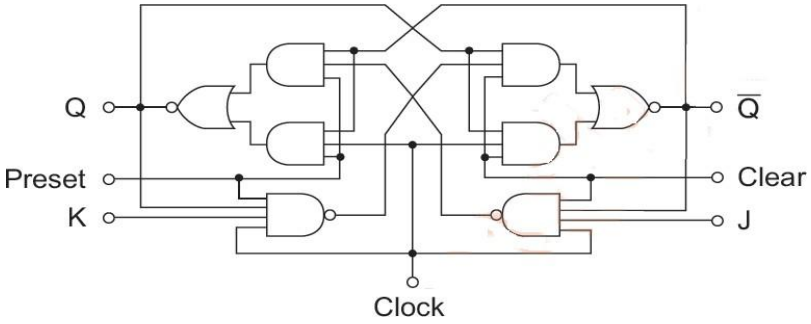


Absolute Maximum Ratings

Item	Symbol	Maximum Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_I	7	V
Power dissipation	P_D	500	mW
Operating temperature	T_A	0-70	℃
Storage temperature	T_S	-65-150	℃
welding temperature	T_W	260	℃,10s

Note: the limit parameter is the limit value that cannot be exceeded under any condition. Once this limit is exceeded, it may cause physical damage such as deterioration of the product. At the same time, the chip can not be guaranteed to work properly when it is close to the limit parameters.

Block Diagram



Function Table

Inputs					Outputs	
Preset	**Clear**	**Clock**	**J**	**K**	**Q**	**$\overline{Q}$**
L	H	×	×	×	H	L
H	L	×	×	×	L	H
L	L	×	×	×	H*	H*
H	H	↓	L	L	Q_0	Q_0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	×	×	Q_0	Q_0

Notes: H; high level, L; low level, X; irrelevant; ↓; transition from high to low level

Q; level of Q before the indicated steady-state input conditions were established.

$\overline{Q}$; complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established.

Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.

*; This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Recommended Operating Conditions

Item		Symbol	Min	Tpy	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	-400	uA
		I_{OL}	—	—	8	mA
Operating temperature		T_{opr}	-20	25	75	℃
Clock frequency		f_{clock}	0	—	30	MHz
Pulse width	CK(Clock High)	t_w	50	—	—	ns
	CLR(Clear Low)	t_w	50	—	—	
Setup time	"H"Data	t_{su}	20↓	—	—	ns
	"L"Data	t_{su}	20↓	—	—	
Hold time		t_h	0↓	—	—	ns

Note: ↓: The arrow indicates the falling edge.

Electrical Characteristics (T_A=25℃, Unless specified)

Item		Symbol	Min	Tpy	Max	Unit	Conditions	
Input voltage		V_{IH}	2	—	—	V		
		V_{IL}	—	—	0.8	V		
Output voltage		V_{OH}	2.7	3.2	—	V	I_{OH}=-400uA	VCC=4.75V,V_{IH}=2V V_{IL}=0.8V
		V_{OL}	—	0.16	0.4	V	I_{OL}=4mA	
			—	0.30	0.5		I_{OL}=8mA	
Input current	J、K	I_{IH}	—	0.1	20	uA	VCC=5.25V, V_I=2.7V	
	Clear		—	0.1	60			
	Clock		—	0.1	80			
	Preset		—	0.1	60			
	J、K	I_{IL}**	—	0.05	-0.4	mA	VCC=5.25V, V_I=0.4V	
	Clear		—	0.13	-0.8			
	Clock		—	0.11	-0.8			
	Preset		—	0.13	-0.8			
	J、K	I_I	—	0.1	0.1	mA	VCC=5.25V, V_I=7V	
	Clear		—	0.1	0.3			
	Clock		—	0.1	0.4			
	Preset		—	0.1	0.3			
Short-circuit output current *		I_{OS}	-20	-32	-100	mA	VCC=5.25V	
Supply current ***		I_{CC}	—	2.5	6	mA	VCC=5.25V	
Input clamp voltage		V_{IK}	—	0.85	-1.5	V	VCC=4.75V, I_I =−18mA	

Notes: * only one output port is short circuited each time, and the short circuit time is not more than one second.

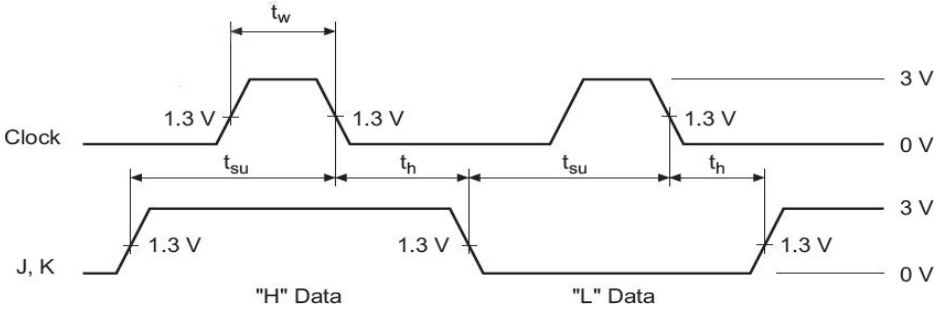
** I_{IL} should not be measured when preset and clear inputs are low at same time.

*** With all outputs open, I_{CC} is measured with the Q and Q outputs high in turn.At the time of measurement, the clock input is grounded.

Switching Characteristics (T_A=25℃, Unless specified)

Item	Symbol	Input	Output	Min	Tpy	Max	Unit	Conditions
Maximum clock frequency	f_{max}			30	45	-	MHz	V_{CC}=5V, C_L=16pF, R_L=2KΩ
Propagation delay time	t_{PLH}	Clear	Qo、$\overline{Q}$ o	—	12	—	ns	
	t_{PHL}	Clock		—	22	—	ns	

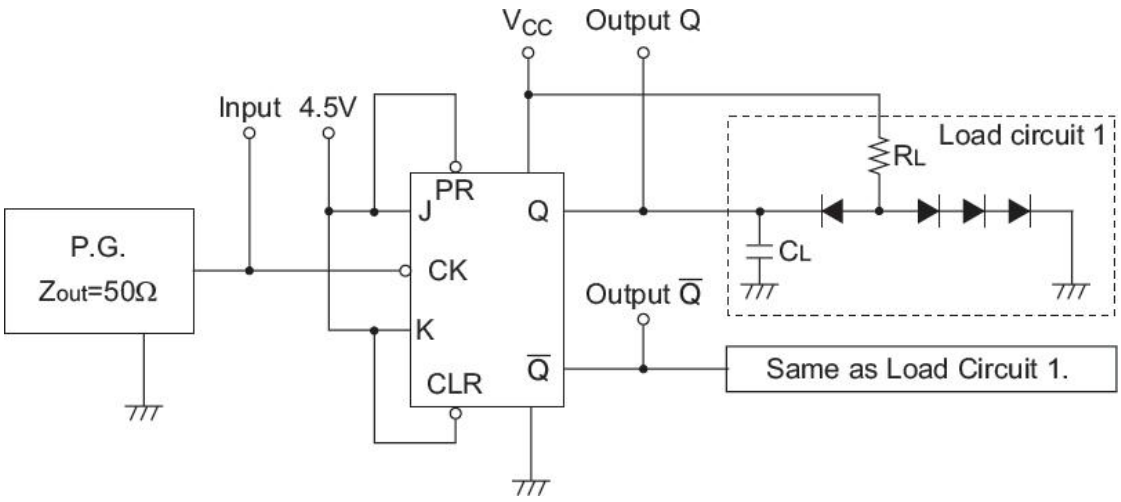
Timing Definition



■ Testing Method

1、f_{max} 、t_{PLH}、t_{PHL} (Clock→Q，$\overline{Q}$)

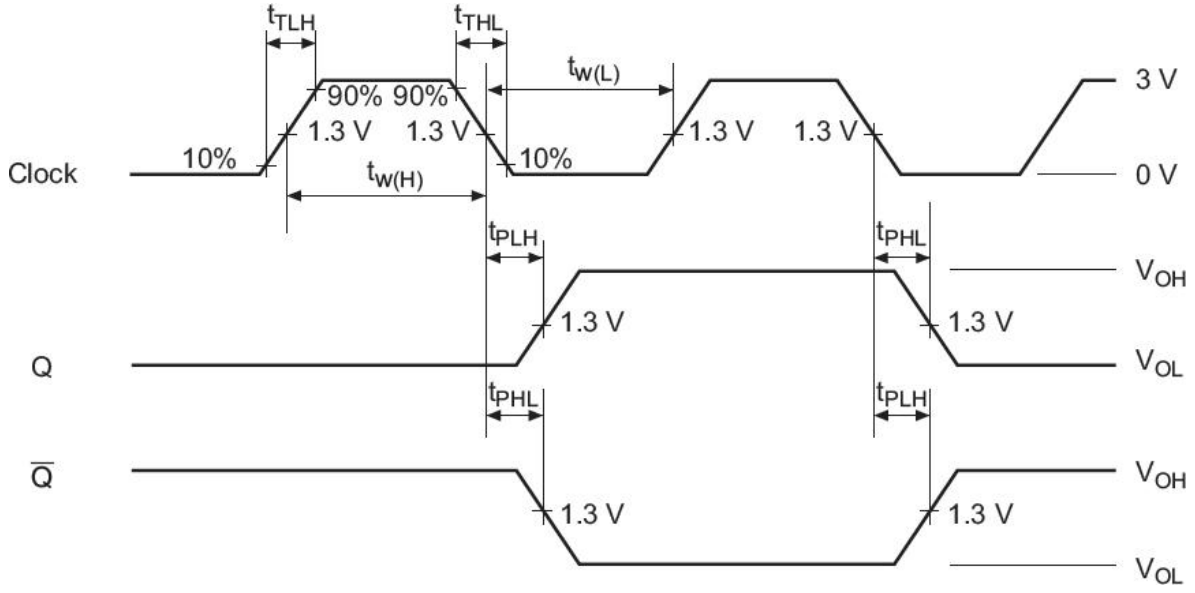
Test Circuit1：



Notes:

1. Only one trigger is tested at a time.
2. the CL capacitor is an external patch capacitor (0603), which is connected to the output pin and the capacitor is near the chip GND.
3. All diode models are 1S2074 (H).

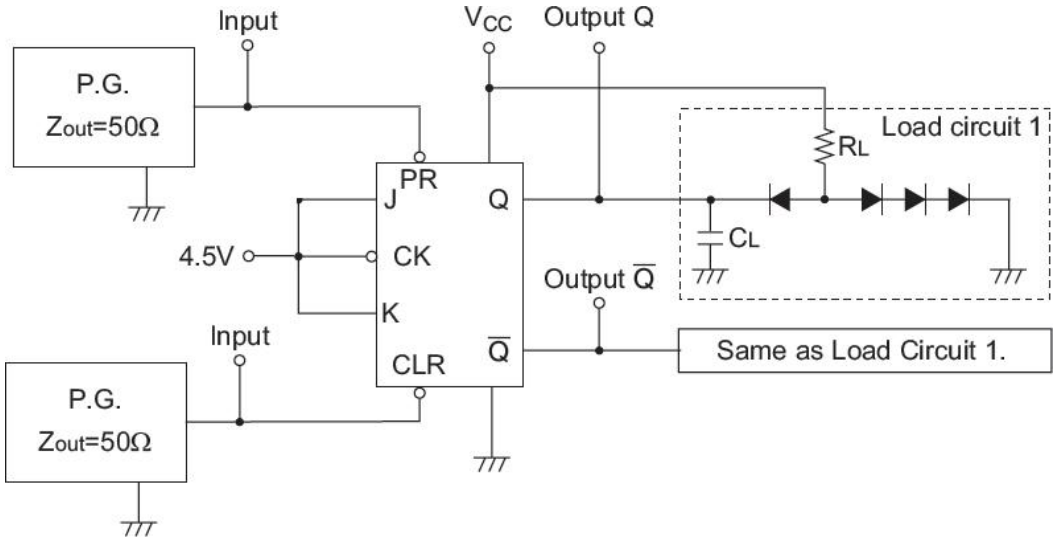
Waveform1：



Note：Clock input pulse； $t_{TLH}=t_{THL}=20$ ns， PRR = 1 MHz， duty cycle = 50% 。

2、t_{PHL} 、t_{PLH} (Clear，Preset→Q, $\overline{Q}$)

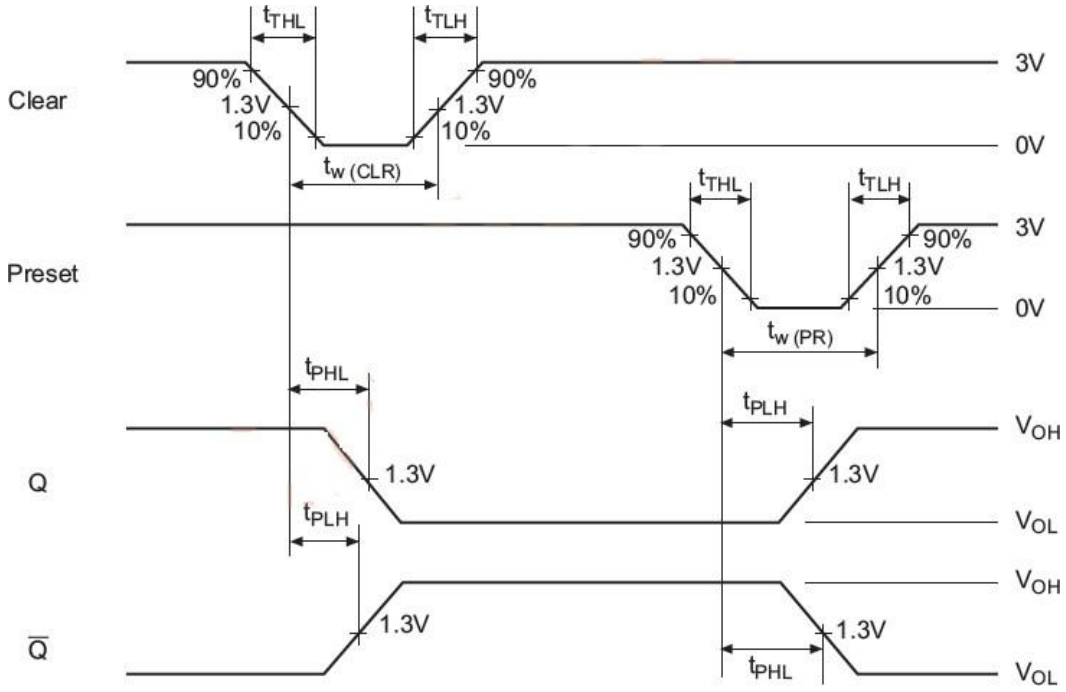
Test Circuit2：



Notes:

1. Only one trigger is tested at a time.
2. the CL capacitor is an external patch capacitor (0603), which is connected to the output pin and the capacitor is near the chip GND.
3. All diode models are 1S2074 (H).

Waveform2：

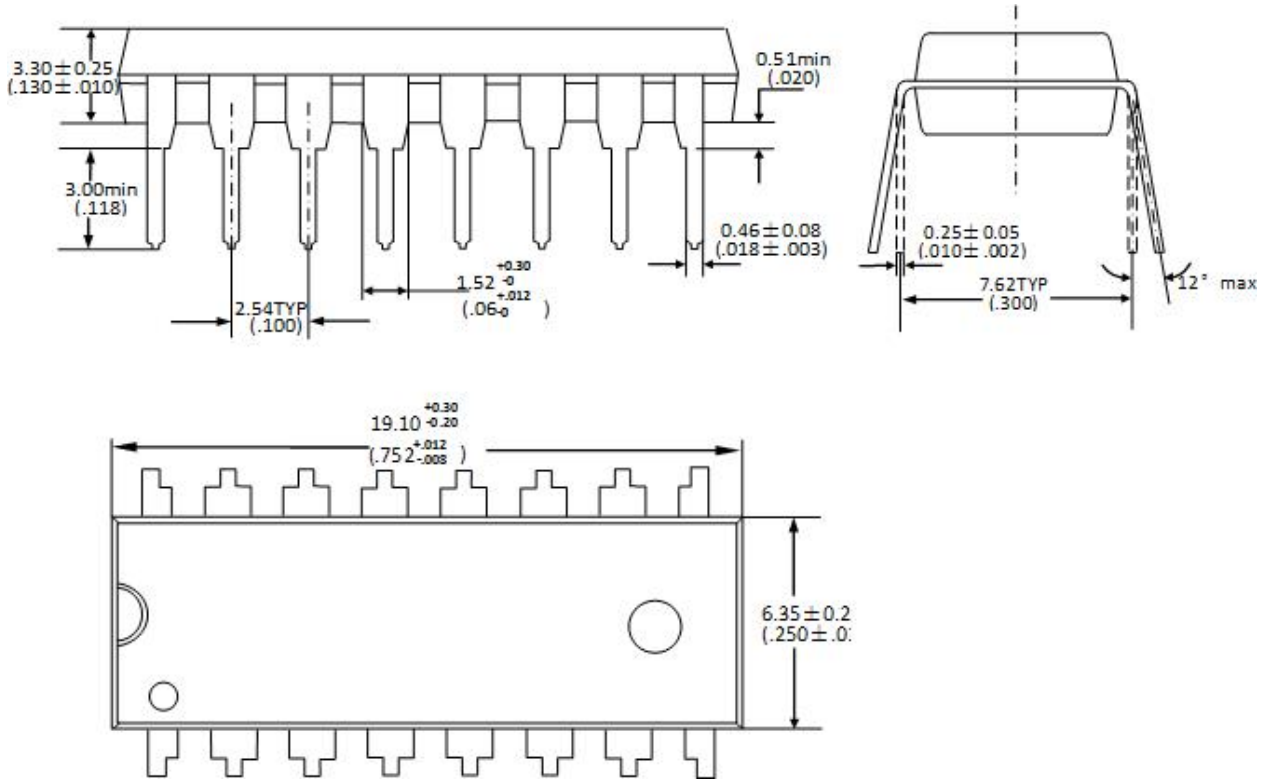


Note： Crear and clock input pulse； $t_{TLH}=t_{THL}=20$ ns， PRR = 1 MHz， duty cycle = 50% 。

■ Package Dimensions

Unit : mm /inch

DIP16



SOP16